USB Charging Port Controller and Power Switch with Load Detection

Check for Samples: TPS2543

FEATURES

- **D+/D– CDP/DCP Modes per USB Battery Charging Specification 1.2**
- **D+/D– Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009**
- **D+/D– Divider Modes 2.0V/2.7V and 2.7/2.0V Compliant with 1A and 2A Apple Mobile Digital Devices**
- **Automatic Selection of D+/D– Mode for an Attached Device**
- **Supports Sleep-Mode Charging and Mouse/Keyboard (Low-Speed Only) Wake Up**
- **Load Detection for Both Power Supply Control in S4/S5 Charging and Port Power Management in all Charge Modes**
- **Compatible with USB 2.0 and 3.0 Power Switch Requirements**
- **73-mΩ (typ) High-Side MOSFET**
- **Adjustable Current-Limit up to 3.0 A (typ)**
- **Operating Range: 4.5 V to 5.5 V**
- **Drop-In Compatible with TPS2540/40A**
- **Available in 16-Pin QFN (3x3) Package**
- **UL Listed and CB File No. E169910**

APPLICATIONS

- **USB Ports (Host and Hubs)**
- **Notebook Desktop PCs**
- **Universal Wall Charging Adapters**

DESCRIPTION

The TPS2543 is a USB charging port controller and power switch with an integrated USB 2.0 high-speed data line (D+/D–) switch. The TPS2543 provides the electrical signatures on D+/D– to support the following charging schemes:

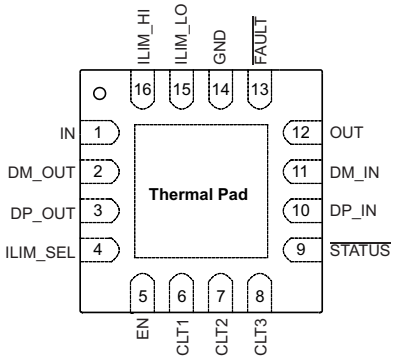
- USB Battery Charging Specification 1.2;
- Chinese Telecom Standard YD/T 1591-2009;
- Divider Mode, Compliant with Apple iPod, iPhone (1A), and iPad (2A) Mobile Digital Devices.(1)

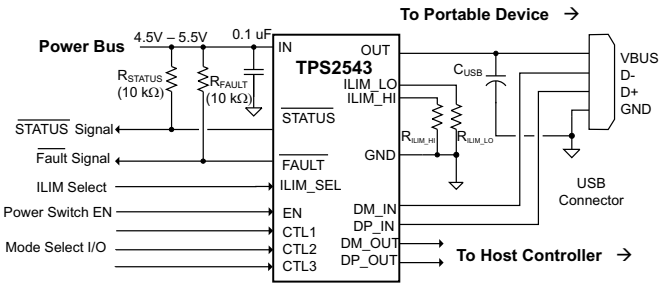
The TPS2543 can be configured to automatically select the D+/D– mode needed to charge an attached device. The TPS2543 provides load detection via the $\overline{\text{STATUS}}$ pin that allows for both power supply control in S4/S5 charging and the ability to manage port power in a multi-port application. Additionally, system wake up (from S3) with a mouse/keyboard (low speed only) is fully supported in the TPS2343.

The TPS2543 73-mΩ power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Two programmable current thresholds provide flexibility for setting current limits and load detect thresholds.

(1) Apple, iPod, iPhone, and iPad are trademarks of Apple Inc., registered in the U.S. and other countries.

TPS2543 RTE PACKAGE AND TYPICAL APPLICATION DIAGRAM





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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	DEVICE	TOP-SIDE MARKING
–40°C to 125°C	QFN16	TPS2543	2543

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, voltages are referenced to GND (unless otherwise noted)

		LIMIT	UNIT
Voltage range	IN, EN, ILIM_LO, ILIM_HI, $\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$, ILIM_SEL, CTL1, CTL2, CTL3, OUT	–0.3 to 7	V
	IN to OUT	–7 to 7	
	DP_IN, DM_IN, DP_OUT, DM_OUT	–0.3 to (IN + 0.3) or 5.7	
Input clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT	±20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT	±100	mA
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	±50	mA
Continuous output current	OUT	Internally limited	
Continuous output sink current	$\overline{\text{FAULT}}$, $\overline{\text{STATUS}}$	25	mA
Continuous output source current	ILIM_LO, ILIM_HI	Internally limited	mA
ESD rating	HBM	2	kV
	HBM wrt GND and each other, DP_IN, DM_IN	8	
	CDM	500	V
Operating junction temperature, T_J		–40 to Internally limited	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2543 RTE (16 PIN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	53.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.4	
θ_{JB}	Junction-to-board thermal resistance	17.2	
ψ_{JT}	Junction-to-top characterization parameter	3.7	
ψ_{JB}	Junction-to-board characterization parameter	20.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

voltages are referenced to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	4.5		5.5	V
	Input voltage, logic-level inputs, EN, CTL1, CTL2, CTL3, ILIM_SEL	0		5.5	V
	Input voltage, data line inputs, DP_IN, DM_IN, DP_OUT, DM_OUT	0		V_{IN}	V
V_{IH}	High-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	1.8			V
V_{IL}	Low-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL			0.8	V
	Continuous current, data line inputs, SDP or CDP mode, DP_IN to DP_OUT, DM_IN to DM_OUT			±30	mA
	Continuous current, data line inputs, BC1.2 DCP mode, DP_IN to DM_IN			±15	mA
I_{OUT}	Continuous output current, OUT	0		2.5	A
	Continuous output sink current, $\overline{FAULT}$, $\overline{STATUS}$	0		10	mA
R_{ILIM_XX}	Current-limit set resistors	16.9		750	kΩ
T_J	Operating virtual junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $–40 ≤ T_J ≤ 125°C$, $4.5\ V ≤ V_{IN} ≤ 5.5\ V$, $V_{EN} = V_{IN}$, $V_{ILIM_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}} = R_{\overline{STATUS}} = 10\ kΩ$, $R_{ILIM_HI} = 20\ kΩ$, $R_{ILIM_LO} = 80.6\ kΩ$. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	On resistance[1]	$T_J = 25°C$, $I_{OUT} = 2\ A$		73	84	mΩ
		$–40°C ≤ T_J ≤ 85°C$, $I_{OUT} = 2\ A$		73	105	
		$–40°C ≤ T_J ≤ 125°C$, $I_{OUT} = 2\ A$		73	120	
t_r	OUT voltage rise time	$V_{IN} = 5\ V$, $C_L = 1\ µF$, $R_L = 100\ Ω$ (see Figure 23 and Figure 24)	0.7	1.0	1.60	ms
t_f	OUT voltage fall time		0.2	0.35	0.5	
t_{on}	OUT voltage turn-on time	$V_{IN} = 5V$, $C_L = 1\ µF$, $R_L = 100\ Ω$ (see Figure 23 and Figure 25)		2.7	4	ms
t_{off}	OUT voltage turn-off time			1.7	3	
I_{REV}	Reverse leakage current	$V_{OUT} = 5.5\ V$, $V_{IN} = V_{EN} = 0\ V$, $–40 ≤ T_J ≤ 85°C$, Measure I_{OUT}			2	µA
DISCHARGE						
R_{DCHG}	OUT discharge resistance	$V_{OUT} = 4\ V$, $V_{EN} = 0\ V$	400	500	630	Ω
t_{DCHG}	OUT discharge hold time	Time $V_{OUT} < 0.7\ V$ (see Figure 26)	205	310	450	ms

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately.

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. $R_{\overline{FAULT}}$ = $R_{\overline{STATUS}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN, ILIMSEL, CTL1, CTL2, CTL3 INPUTS						
	Input pin rising logic threshold voltage		1	1.35	1.70	V
	Input pin falling logic threshold voltage		0.85	1.15	1.45	
	Hysteresis(2)			200		mV
	Input current	Pin voltage = 0 V or 5.5 V	–0.5		0.5	µA
ILIMSEL CURRENT LIMIT						
I_{OS}	OUT short circuit current limit(3)	V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 210 kΩ	205	240	275	mA
		V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 80.6 kΩ	575	625	680	
		V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 22.1 kΩ	2120	2275	2430	
		V_{ILIM_SEL} = V_{IN}, R_{ILIM_HI} = 20 kΩ	2340	2510	2685	
		V_{ILIM_SEL} = V_{IN}, R_{ILIM_HI} = 16.9 kΩ	2770	2970	3170	
t_{IOS}	Response time to OUT short-circuit(2)	V_{IN} = 5.0 V, R = 0.1Ω, lead length = 2 inches (see Figure 27)		1.5		µs
SUPPLY CURRENT						
I_{IN_OFF}	Disabled IN supply current	V_{EN} = 0 V, V_{OUT} = 0 V, –40 ≤ T_J ≤ 85°C			2	µA
I_{IN_ON}	Enabled IN supply current	V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0 V or V_{IN}, V_{ILIM_SEL} = 0 V		155	210	µA
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0V, V_{ILIM_SEL} = V_{IN}		175	230	
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = VIN, V_{ILIM_SEL} = V_{IN}		185	240	
		V_{CTL1} = 0V, V_{CTL2} = V_{CTL3} = V_{IN}		205	260	
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis(2)			100		mV
$\overline{FAULT}$						
	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V			1	µA
	Over current $\overline{FAULT}$ rising and falling deglitch		5	8.2	12	ms
$\overline{STATUS}$						
	Output low voltage	$I_{\overline{STATUS}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{STATUS}}$ = 6.5 V			1	µA
THERMAL SHUTDOWN						
	Thermal shutdown threshold		155			°C
	Thermal shutdown threshold in current-limit		135			
	Hysteresis(2)			20		

(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately.

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ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH

Unless otherwise noted: $-40 \le T_J \le 125°C$, $4.5\ V \le V_{IN} \le 5.5\ V$, $V_{EN} = V_{IN}$, $V_{ILIM_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}} = R_{\overline{STATUS}} = 10\ k\Omega$, $R_{ILIM_HI} = 20\ k\Omega$, $R_{ILIM_LO} = 80.6\ k\Omega$, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
	DP/DM switch on resistance	$V_{DP/DM_OUT} = 0\ V$, $I_{DP/DM_IN} = 30\ mA$		2	4	Ω
		$V_{DP/DM_OUT} = 2.4\ V$, $I_{DP/DM_IN} = -15\ mA$		3	6	
	Switch resistance mismatch between DP / DM channels	$V_{DP/DM_OUT} = 0\ V$, $I_{DP/DM_IN} = 30\ mA$		0.05	0.15	Ω
		$V_{DP/DM_OUT} = 2.4\ V$, $I_{DP/DM_IN} = -15\ mA$		0.05	0.15	
	DP/DM switch off-state capacitance(1)	$V_{EN} = 0\ V$, $V_{DP/DM_IN} = 0.3\ V$, $V_{ac} = 0.6\ V_{pk-pk}$, $f = 1\ MHz$		3	3.6	pF
	DP/DM switch on-state capacitance(2)	$V_{DP/DM_IN} = 0.3\ V$, $V_{ac} = 0.6\ V_{pk-pk}$, $f = 1\ MHz$		5.4	6.2	pF
O_{IRR}	Off-state isolation(3)	$V_{EN} = 0\ V$, $f = 250\ MHz$		33		dB
X_{TALK}	On-state cross channel isolation(3)	$f = 250\ MHz$		52		dB
	Off state leakage current	$V_{EN} = 0\ V$, $V_{DP/DM_IN} = 3.6\ V$, $V_{DP/DM_OUT} = 0\ V$, measure I_{DP/DM_OUT}		0.1	1.5	µA
BW	Bandwidth (–3dB)(3)	$R_L = 50\ \Omega$		2.6		GHz
t_{pd}	Propagation delay(3)			0.25		ns
t_{SK}	Skew between opposite transitions of the same port ($t_{PHL} - t_{PLH}$)			0.1	0.2	ns

(1) The resistance in series with the parasitic capacitance to GND is typically 250 Ω.
(2) The resistance in series with the parasitic capacitance to GND is typically 150 Ω
(3) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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ELECTRICAL CHARACTERISTICS, CHARGING CONTROLLER

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = 0 V, V_{CTL2} = V_{CTL3} = V_{IN}. $R_{\overline{FAULT}}$ = $R_{\overline{STATUS}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORTED MODE		**VCTL1 = VIN, VCTL2 = VCTL3 = 0V**				
	DP_IN / DM_IN shorting resistance			125	200	Ω
DIVIDER1 MODE						
	DP_IN Divider1 output voltage		1.9	2.0	2.1	V
	DM_IN Divider1 output voltage		2.57	2.7	2.84	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
DIVIDER2 MODE		**IOUT = 1A**				
	DP_IN Divider2 output voltage		2.57	2.7	2.84	V
	DM_IN Divider2 output voltage		1.9	2.0	2.1	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
CHARGING DOWNSTREAM PORT		**VCTL1 = VCTL2 = VCTL3 = VIN**				
V_{DM_SRC}	DM_IN CDP output voltage	V_{DP_IN} = 0.6 V, –250 µA < I_{DM_IN} < 0 µA	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window thresholdfor V_{DM_SRC} activation		0.25		0.4	V
	Hysteresis(1)			50		mV
V_{LGC_SRC}	DP_IN rising upper window thresholdfor V_{DM_SRC} de-activation		0.8		1	V
	hysteresis(1)			100		mV
I_{DP_SINK}	DP_IN sink current	V_{DP_IN} = 0.6 V	40	70	100	µA
LOAD DETECT – NON POWER WAKE		**VCTL1 = VCTL2 = VCTL3 = VIN**				
I_{LD}	IOUT rising load detect current threshold		635	700	765	mA
	hysteresis(1)			50		mA
t_{LD_SET}	Load detect set time		140	200	275	ms
	Load detect reset time		1.9	3	4.2	s
LOAD DETECT – POWER WAKE		**VCTL1 = VCTL2 = 0V, VCTL3 = VIN**				
I_{OS_PW}	Power wake short circuit current limit		32	55	78	mA
	I_{OUT} falling power wake reset current detection threshold		23	45	67	mA
	Reset current hysteresis(1)			5		mA
	Power wake reset time		10.7	15	20.6	s

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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TYPICAL CHARACTERISTICS

POWER SWITCH ON RESISTANCE vs TEMPERATURE

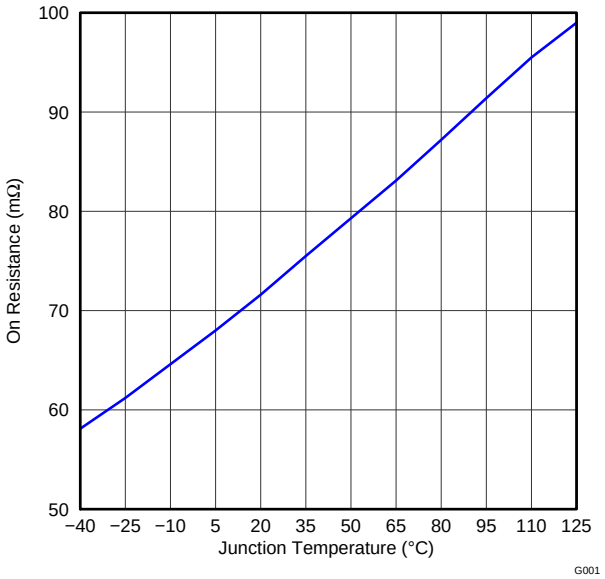


Figure 1.

REVERSE LEAKAGE CURRENT vs TEMPERATURE

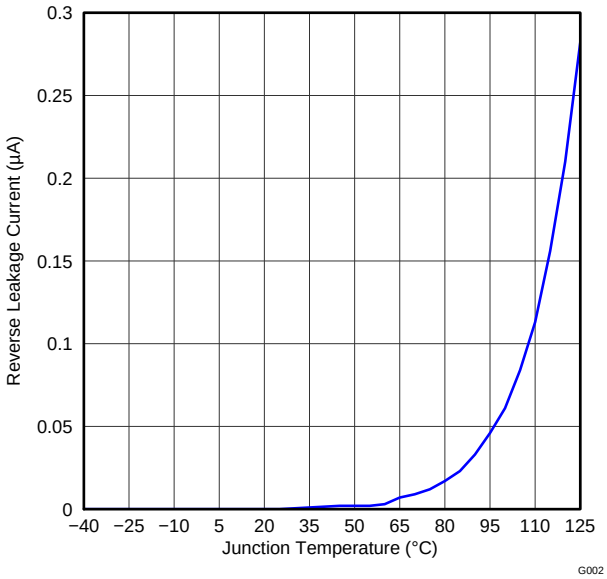


Figure 2.

OUT DISCHARGE RESISTANCE vs TEMPERATURE

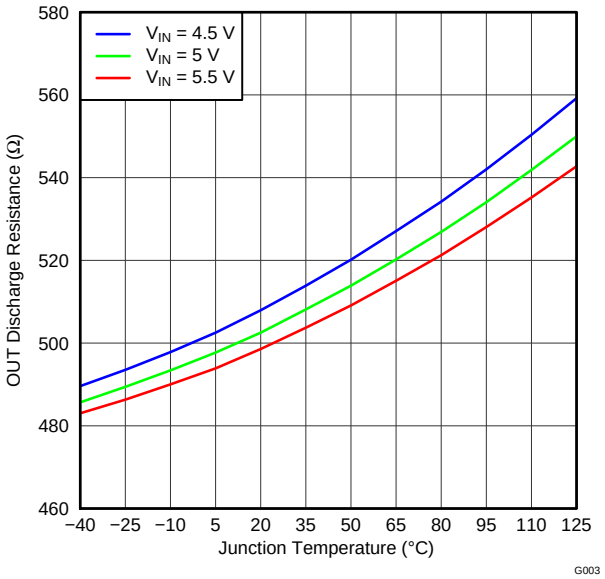


Figure 3.

OUT SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

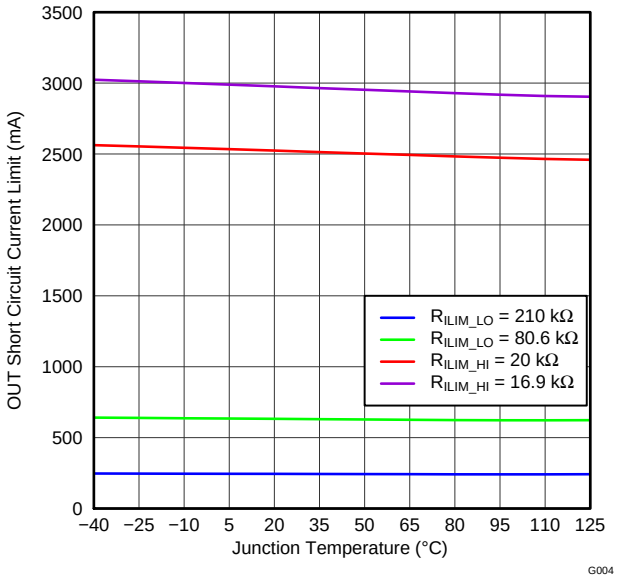


Figure 4.

TYPICAL CHARACTERISTICS (continued)

DISABLED IN SUPPLY CURRENT vs TEMPERATURE

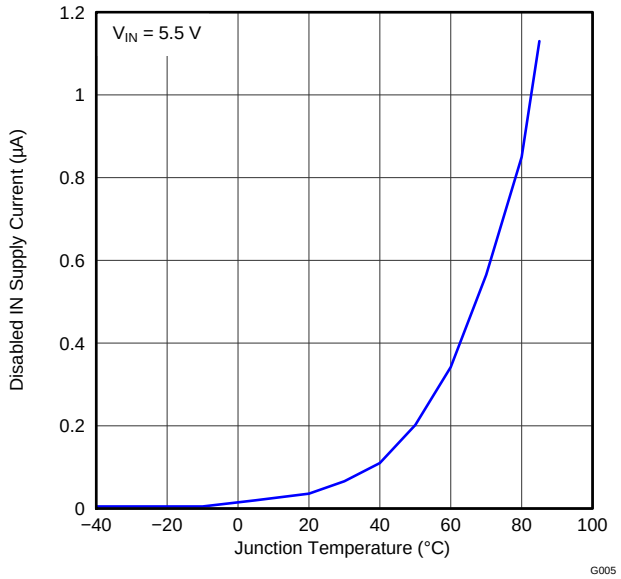


Figure 5.

ENABLED IN SUPPLY CURRENT - SDP vs TEMPERATURE

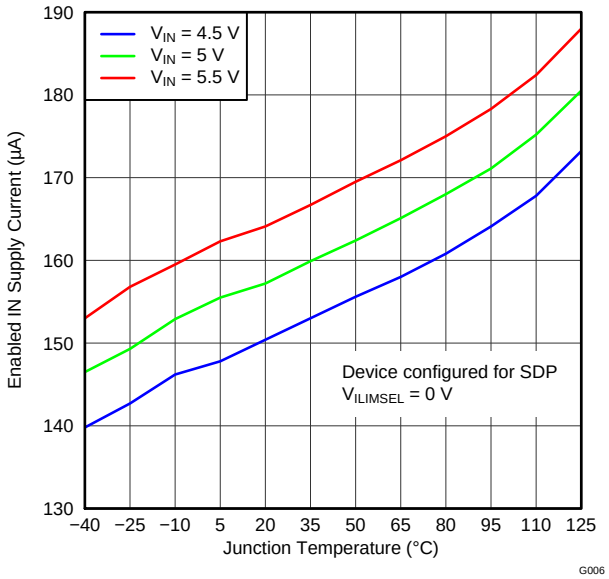


Figure 6.

ENABLED IN SUPPLY CURRENT - CDP vs TEMPERATURE

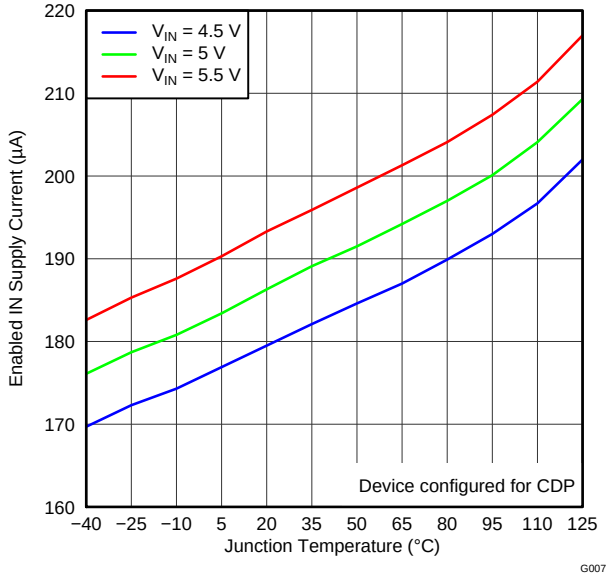


Figure 7.

ENABLED IN SUPPLY CURRENT - DCP AUTO vs TEMPERATURE

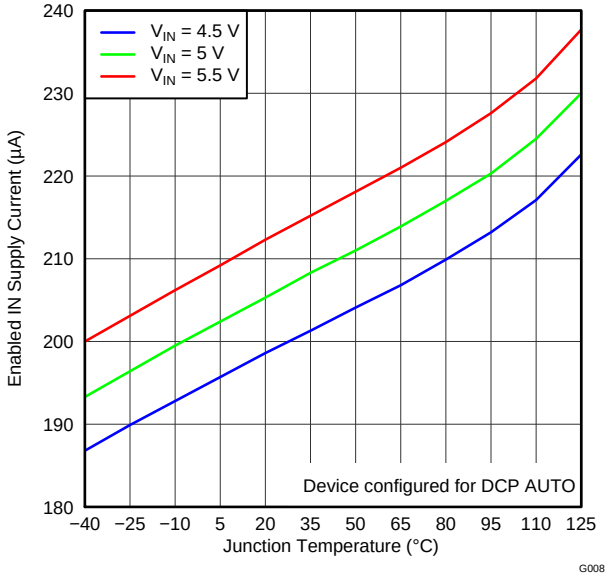


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

$\overline{\text{STATUS}}$ AND $\overline{\text{FAULT}}$ OUTPUT LOW VOLTAGE vs SINKING CURRENT

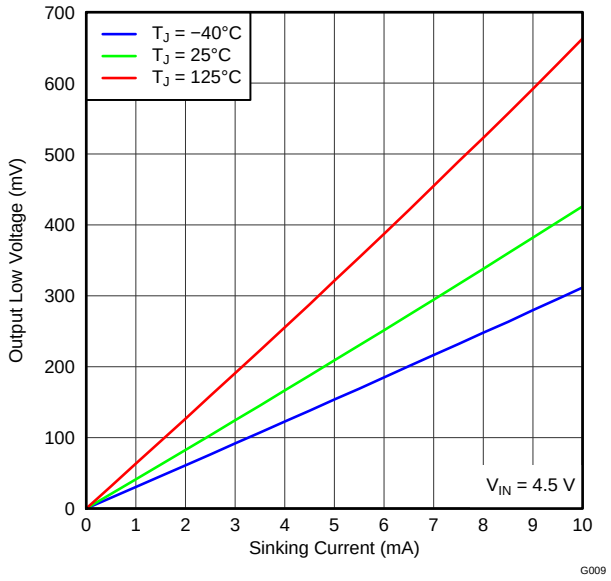


Figure 9.

DATA TRANSMISSION CHARACTERISTICS vs FREQUENCY

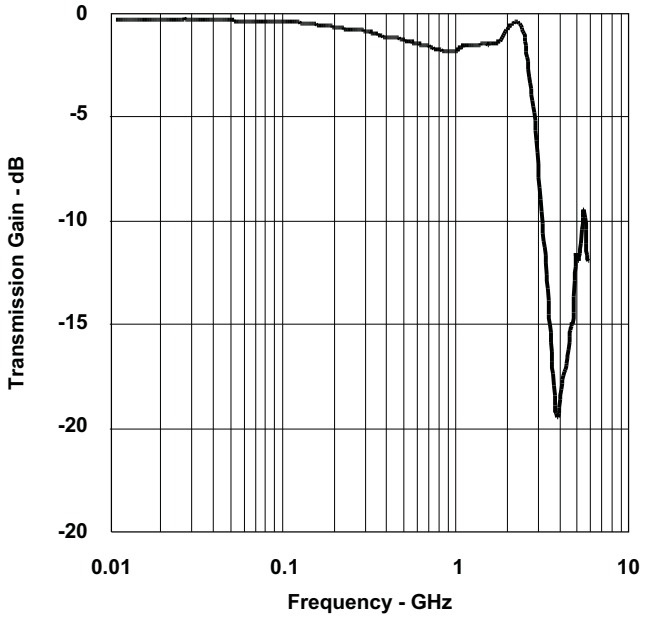


Figure 10.

OFF STATE DATA SWITCH ISOLATION vs FREQUENCY

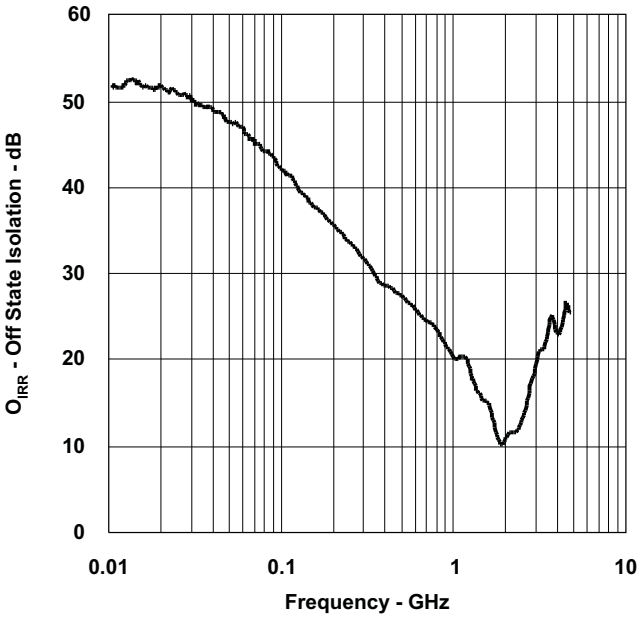


Figure 11.

ON STATE CROSS-CHANNEL ISOLATION vs FREQUENCY

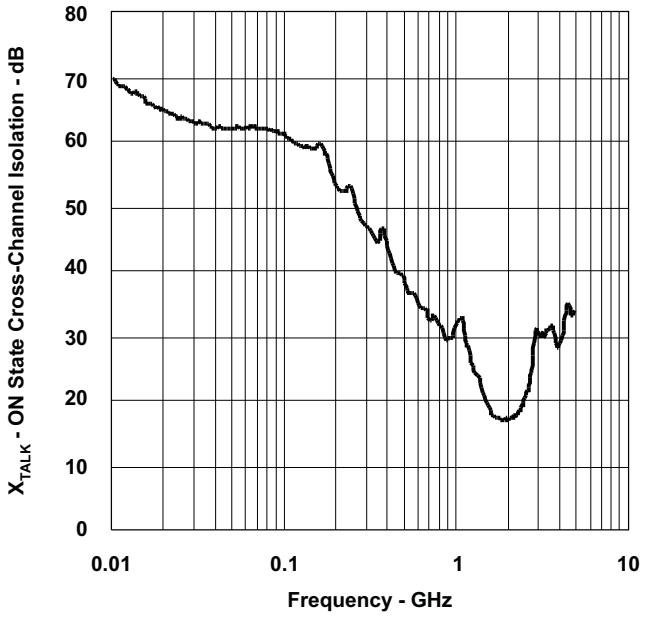


Figure 12.

TYPICAL CHARACTERISTICS (continued)

EYE DIAGRAM USING USB COMPLIANCE TEST PATTERN (with no switch)

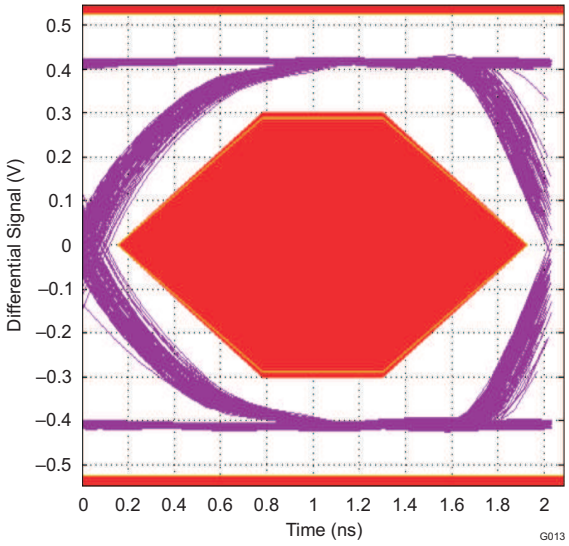


Figure 13.

EYE DIAGRAM USING USB COMPLIANCE TEST PATTERN (with data switch)

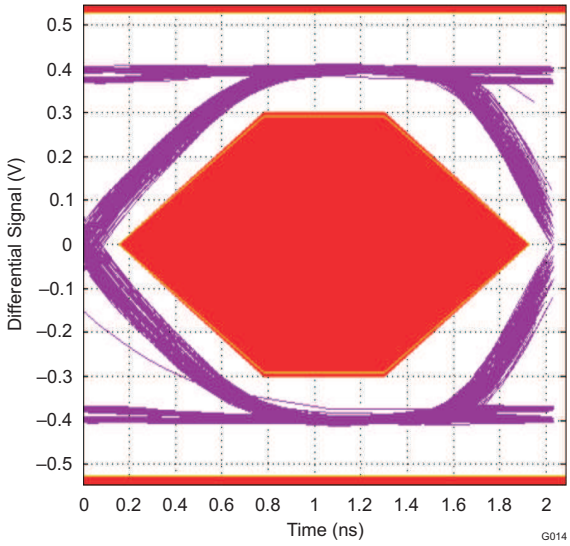


Figure 14.

I_{OUT} RISING LOAD DETECT THRESHOLD AND OUT SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

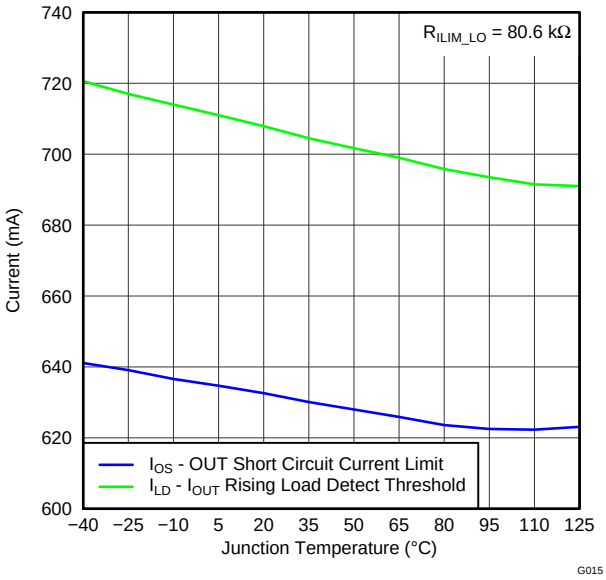


Figure 15.

LOAD DETECT SET TIME vs TEMPERATURE

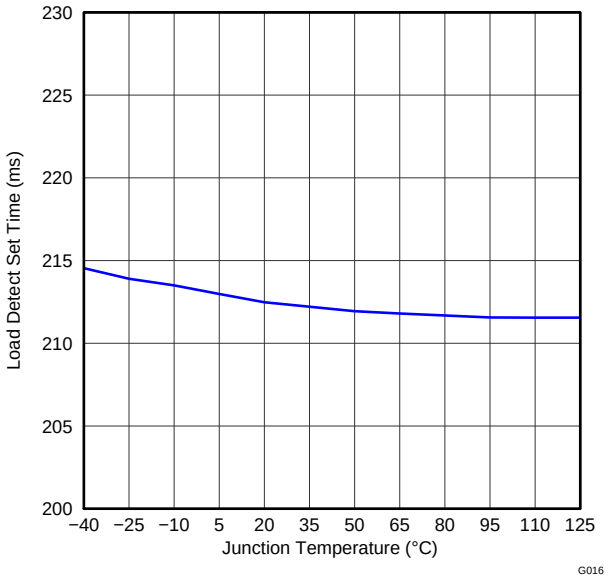


Figure 16.

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TYPICAL CHARACTERISTICS (continued)

POWER WAKE CURRENT LIMIT vs TEMPERATURE

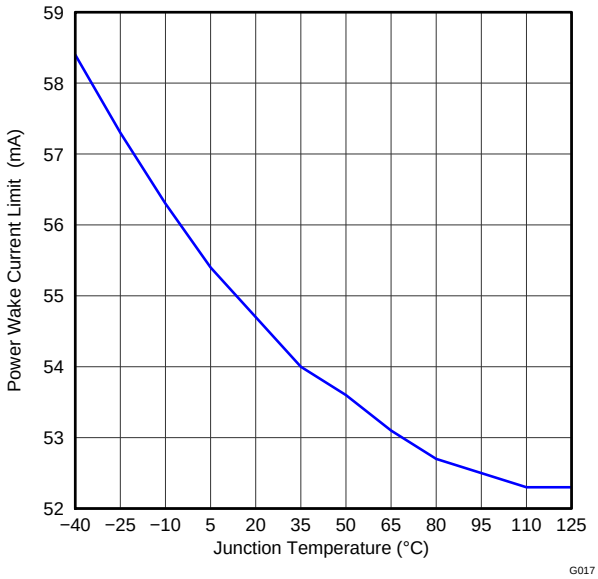


Figure 17.

TURN-ON RESPONSE

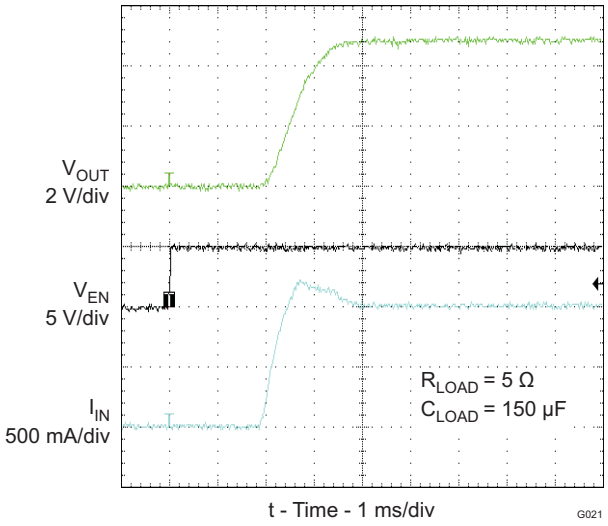


Figure 18.

TURN-OFF RESPONSE

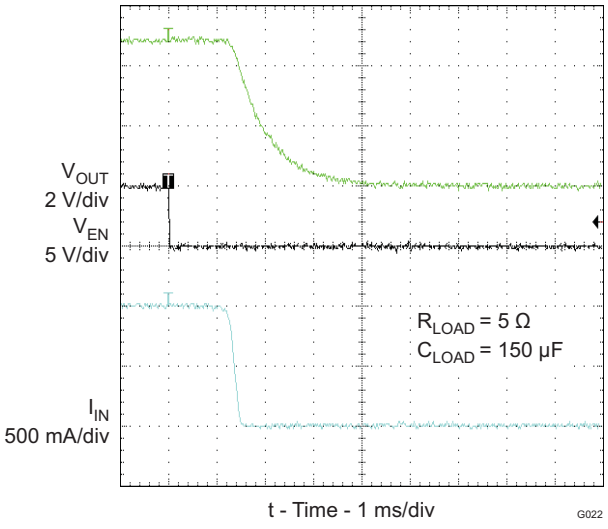


Figure 19.

DEVICE ENABLED INTO SHORT CIRCUIT

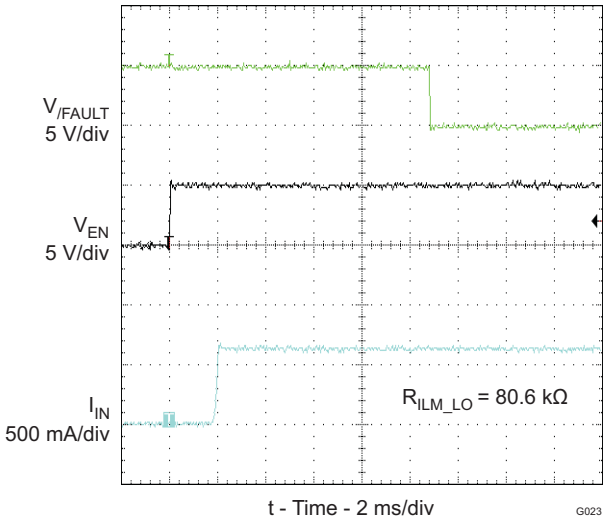


Figure 20.

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TYPICAL CHARACTERISTICS (continued)

DEVICE ENABLED INTO SHORT CIRCUIT - THERMAL CYCLING

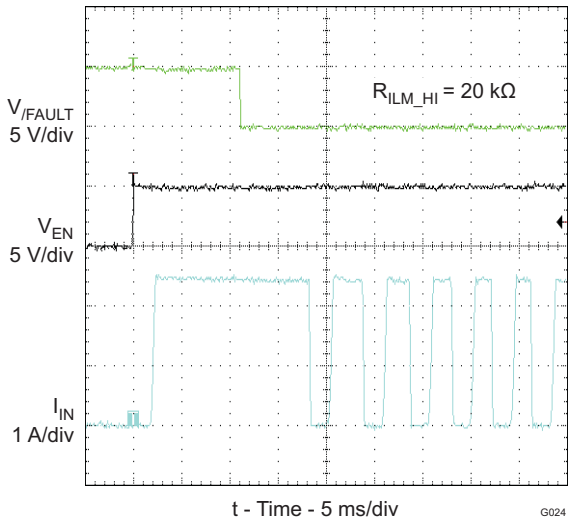


Figure 21.

SHORT CIRCUIT to FULL LOAD RECOVERY

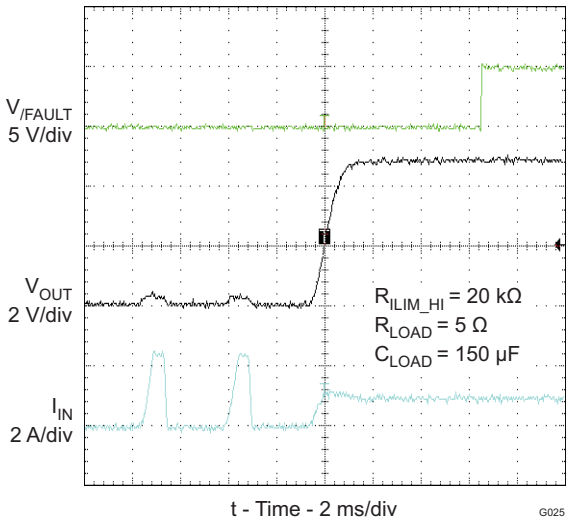


Figure 22.

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PARAMETER MEASUREMENT DESCRIPTION

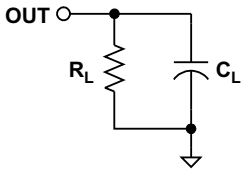


Figure 23. OUT Rise/Fall Test Load

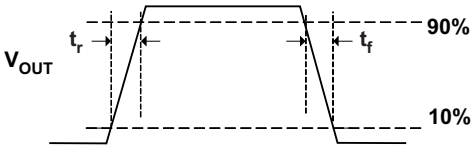


Figure 24. Power-On and Off Timing

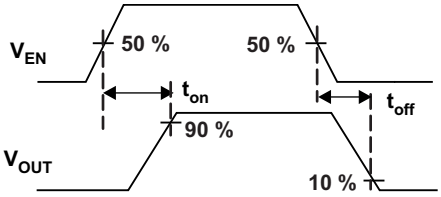


Figure 25. Enable Timing, Active High Enable

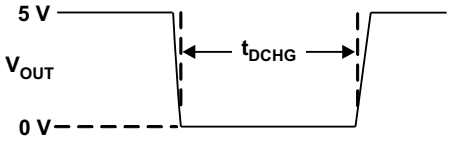


Figure 26. OUT Discharge During Mode Change

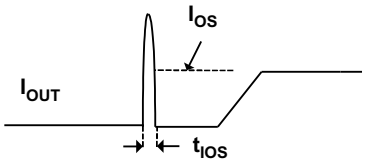
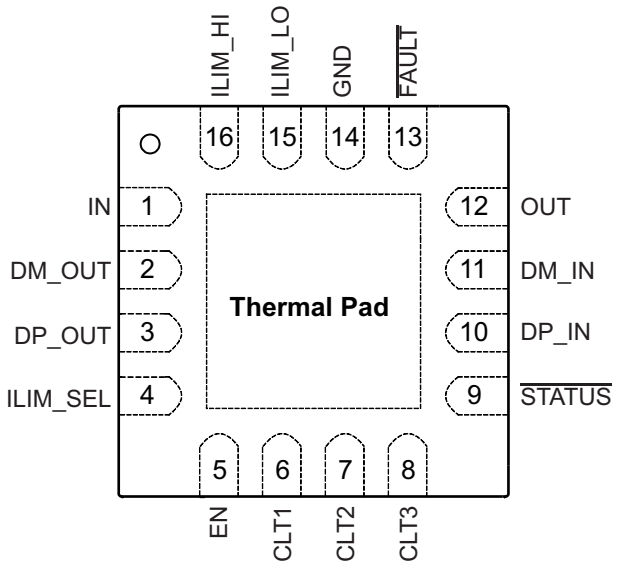


Figure 27. Output Short Circuit Parameters

DEVICE INFORMATION

TPS2543 RTE PACKAGE
(Top View)



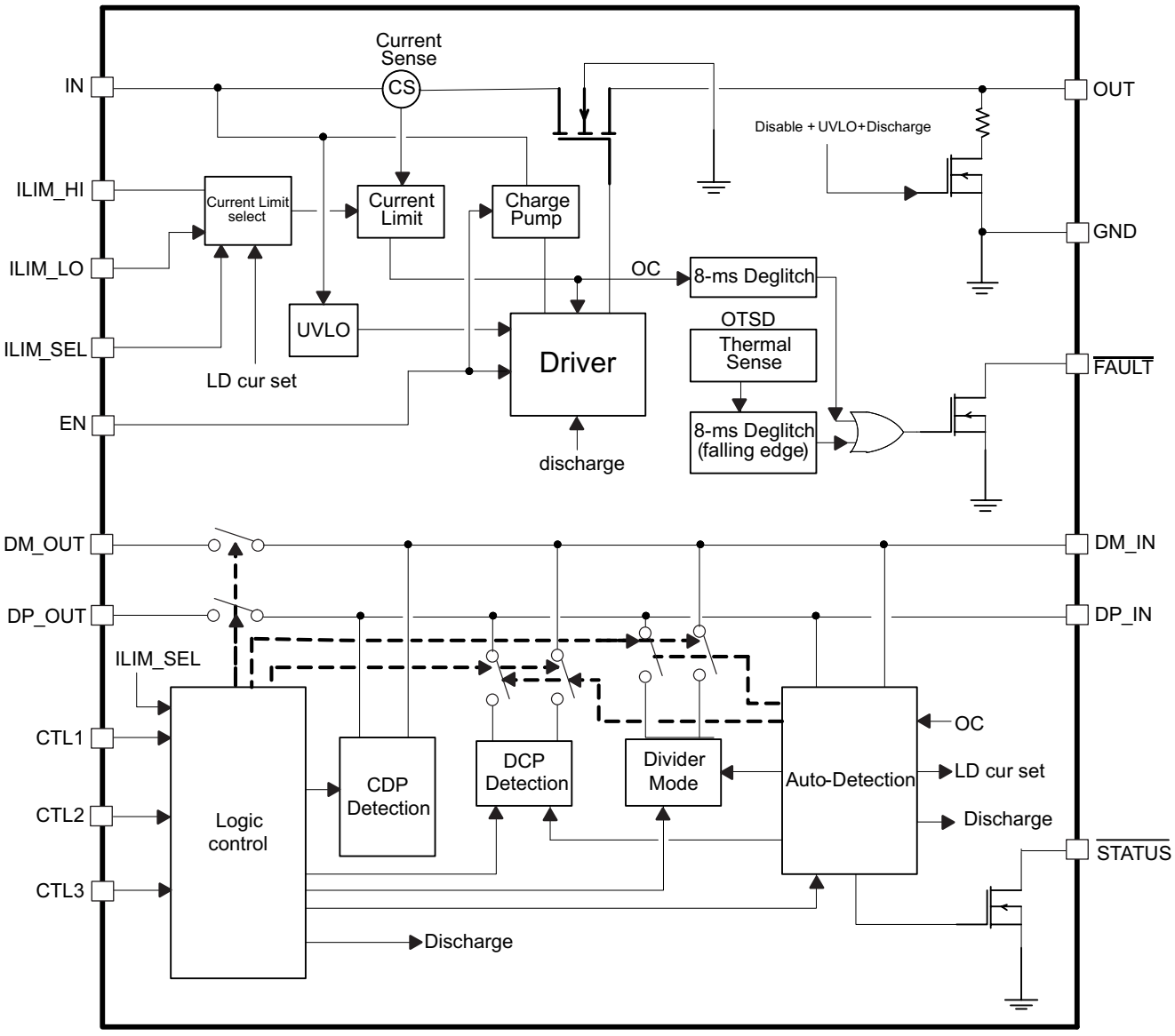
PIN FUNCTIONS

NO.	NAME	TYPE(1)	DESCRIPTION
1	IN	P	Input voltage and supply voltage; connect 0.1 µF or greater ceramic capacitor from IN to GND as close to the device as possible
2	DM_OUT	I/O	D– data line to USB host controller
3	DP_OUT	I/O	D+ data line to USB host controller
4	ILIM_SEL	I	Logic-level input signal used to control the charging mode, current limit threshold, and load detection; see the control truth table
5	EN	I	Logic-level input for turning the power switch and the signal switches on/off; logic low turns off the signal and power switches and holds OUT in discharge.
6	CTL1	I	Logic-level inputs used to control the charging mode and the signal switches; see the control truth table
7	CTL2	I	
8	CTL3	I	
9	$\overline{\text{STATUS}}$	O	Active-low open-drain output, asserted in load detection conditions
10	DP_IN	I/O	D+ data line to downstream connector
11	DM_IN	I/O	D– data line to downstream connector
12	OUT	P	Power-switch output
13	$\overline{\text{FAULT}}$	O	Active-low open-drain output, asserted during over-temperature or current limit conditions
14	GND	P	Ground connection
15	ILIM_LO	I	External resistor used to set the low current-limit threshold and the load detection current threshold. A resistor to ILIM_LO is optional; see Current-Limit Settings in DETAILED DESCRIPTION.
16	ILIM_HI	I	External resistor used to set the high current-limit threshold
NA	PowerPAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect to GND plane.

(1) G = Ground, I = Input, O = Output, P = Power

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FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Overview

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5 V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, USB host ports following the USB 2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and may request more current in 100 mA unit steps up to 500 mA. The host may grant or deny based on the available current.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector. One common difficulty has resulted from this. As USB charging has gained popularity, the 500 mA minimum defined by USB 2.0 or 900 mA for USB 3.0 has become insufficient for many handset and personal media players which need a higher charging rate. Wall adapters can provide much more current than 500mA/900mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500mA/900mA minimum defined by USB 2.0/3.0 while still using a single micro-USB input connector.

The TPS2543 supports three of the most common protocols:

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode

All three methods have similarities and differences, but the biggest commonality is that all three define three types of charging ports that provide charging current to client-side devices. These charging ports are defined as:

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a Charging Port as a downstream facing USB port that provides power for charging portable equipment.

Table 1 shows the differences between these ports according to BC1.2 .

Table 1. Operating Modes

PORT TYPE	SUPPORT USB 2.0 COMMUNICATION	MAX. ALLOWABLE CURRENT DRAW BY PORTABLE DEVICE (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

BC1.2 defines the protocol necessary to allow portable equipment to determine what type of port it is connected to so that it can allot its maximum allowable current draw. The hand-shaking process has two steps. During step one, the primary detection, the portable equipment outputs a nominal 0.6-V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V. The second step, the secondary detection, is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

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Standard Downstream Port (SDP) USB 2.0/USB 3.0

An SDP is a traditional USB port that follows USB 2.0/3.0 protocol and supplies a minimum of 500 mA/900 mA per port. USB 2.0/3.0 communications is supported, and the host controller must be active to allow charging.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process is two steps. During step one the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

The second step is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

Dedicated Charging Port (DCP)

A DCP only provides power and does not provide data connection to an upstream port. A DCP is identified by the electrical characteristics of its data lines. The TPS2543 emulates two common charging standards namely, BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, and one brand unique DCP charging scheme which will be referred to as Divider scheme.

DCP BC 1.2 and YD/T 1591-2009

Both standards defines that the D+ and D- data lines should be shorted together with a maximum series impedance of 200 Ω. This is shown in Figure 28.

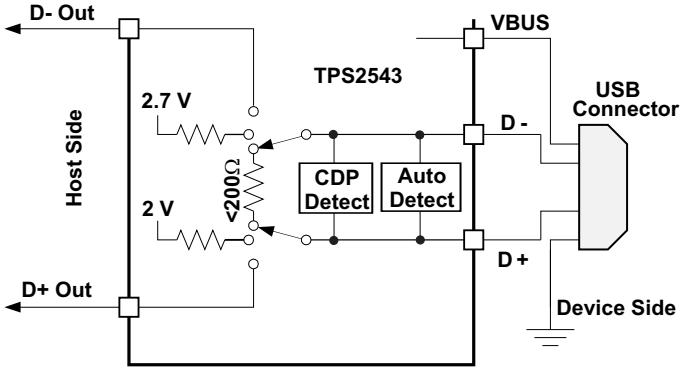


Figure 28. DCP Supporting BC 1.2/YD/T 1591-2009

DCP Divider Charging Scheme

There are two Divider charging schemes supported by the device, Divider 1 and Divider 2 as shown in Figure 29 and Figure 30. In Divider 1 charging scheme the device applies 2.0V and 2.7V to D+ and D- data line respectively. This is reversed in Divider 2 mode shown in Figure 30.

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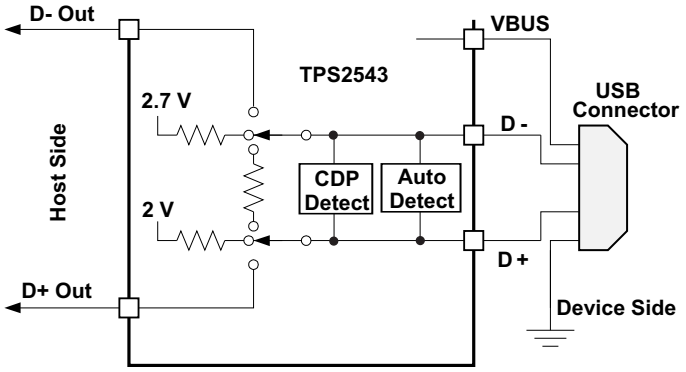


Figure 29. DCP Divider 1 Scheme

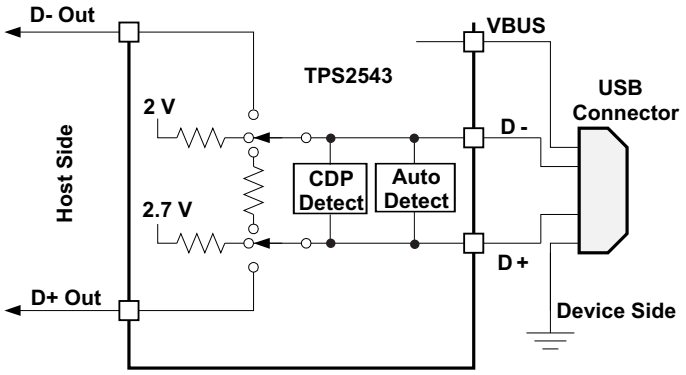


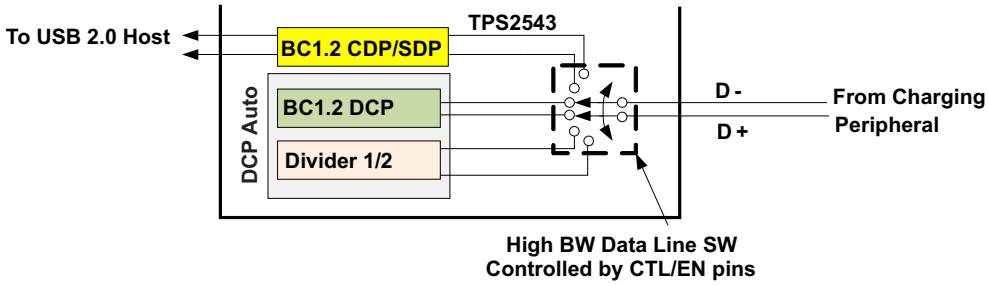
Figure 30. Divider 2 Scheme

Divider 1 voltage configuration is required for 1A (max) iPhone device charging while Divider 2 will allow fast charging iPAD devices at 2.1A.

DCP Auto Mode

The TPS2543 integrates an auto-detect feature that supports the above DCP schemes. It starts in Divider 1 scheme, if a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2543 responds by discharging OUT, turning back ON the power switch and operating in BC1.2 DCP. It then stays in that mode until the device releases the data line, in which case it goes back to Divider Mode.

Also, the TPS2543 will automatically switch between the Divider 1 and Divider 2 schemes based on charging current drawn by the connected device. Initially the device will set the data lines to Divider 1 mode. If charging current of >750mA is measured by the TPS2543 it switches to Divider 2 scheme and test to see if the peripheral device will still charge at a high current. If it does then it stays in Divider 2 scheme otherwise it will revert to Divider 1 scheme.



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DCP Forced Shorted / DCP Forced Divider 1

In this mode the device is permanently set to one of the DCP schemes (BC 1.2/ YD/T 1591-2009 or Divider 1) as commanded by its control pin setting per device truth table.

High-Bandwidth Data Line Switch

The TPS2543 passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes. The EN input also needs to be at logic High for the data line switches to be enabled.

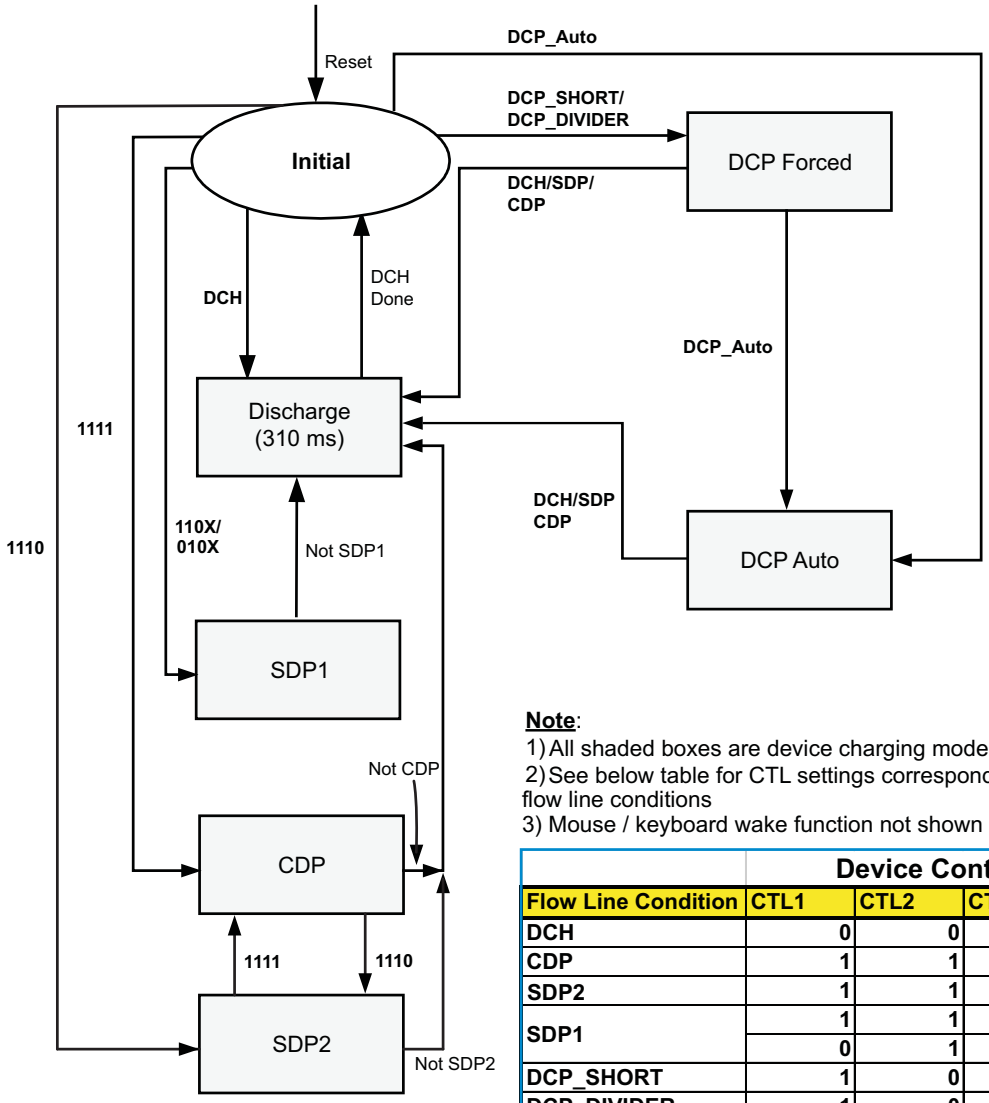
NOTE

1. While in CDP mode, the data switches are ON even while CDP handshaking is occurring.
2. The data line switches are OFF if EN or all CTL pins are held low, or if in DCP mode. They are not automatically turned off if the power switch (IN to OUT) is in current limit.
3. The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the TPS2543.

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Device Operation

Please refer to the simplified device state diagram in Figure 31. Power-on-reset (POR) holds device in initial state while output is held in discharge mode. Any POR event will take the device back to initial state. After POR clears, device goes to the next state depending on the CTL lines as shown in Figure 31.



Note:
1) All shaded boxes are device charging modes
2) See below table for CTL settings corresponding to flow line conditions
3) Mouse / keyboard wake function not shown

	Device Control Pins			
Flow Line Condition	**CTL1**	**CTL2**	**CTL3**	**ILIM_SEL**
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Figure 31. TPS2543 Charging States

Output Discharge

To allow a charging port to renegotiate current with a portable device, TPS2543 uses the OUT discharge function. It proceeds by turning off the power switch while discharging OUT, then turning back on the power switch to reassert the OUT voltage. This discharge function is automatically applied as shown in device state diagram.

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Mouse/Key Board Wake Function

The TPS2543 supports ***low speed*** HID (human interface device like mouse/key board) wake function. It does not support Full Speed HID. There are two scenarios under which wake on mouse is supported by the TPS2543. They are:

1. CDP/SDP2 (111X) to DCP/Auto (011X)
2. SDP1 (010X) to DCP/Auto (011X)

Below description illustrates wake on mouse operation for scenario 1, same holds true for scenario 2.

When a low speed compliant device is attached to the TPS2543, charging port D- line will be pulled high in its idle state (mouse/keyboard not activated). TPS2543 will monitor D- data line continuously. When device is in CDP (1111) or SDP2 (1110) or SDP1 (010X) mode and system is commanded to go to sleep state, the device CTL setting is also changed. Assuming it is changed to DCP/Auto, 011X, having previously detected a HID attachment the device will simply ignore the command to go to DCP/Auto mode and stay in CDP/SDP2 state to support wake on mouse function. When the USB low speed HID is activated (clicked) while system is in S3 (sleep) mode the high speed switch within the TPS2543 allows the transfer of signal from the HID device to the USB host. The USB host subsequently wakes the system and changes CTL setting of the TPS2543 back to CDP/SDP2 mode. Activating (clicking) the low speed device makes the D- data line go back low momentarily, this triggers an internal timer within the TPS2543 to count down. If after ~64ms the CTL lines are still set at 011X (DCP/Auto) the device will immediately switch to DCP/Auto mode and disconnect the mouse from the host. To prevent this, the CTL setting must be made in less then 64 ms after HID device activation otherwise mouse/KB function will be lost. See Figure 32 scope plot for an event sequence where mouse connection is maintained at wake.

Mouse Wake from Sleep

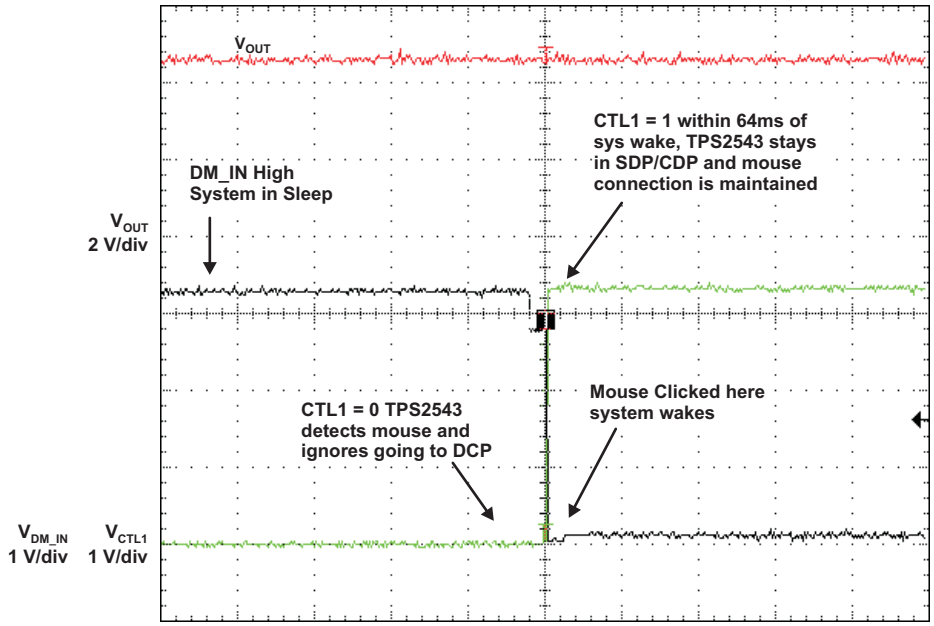


Figure 32. Mouse Wake from Sleep Scope Plot

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Device Truth Table (TT)

Device TT lists all valid bias combinations for the three control pins CTL1-3 and ILIM_SEL pin and their corresponding charging mode. It is important to note that the TT *purposely* omits matching charging modes of the TPS2543 with global power states (S0-S5) as device is agnostic to system power states. The TPS2543 monitors its CTL inputs and will transition to whatever charging state it is commanded to go to (except when LS HID device is detected). For example if sleep charging is desired when system is in standby or hibernate state then user must set TPS2543 CTL pins to correspond to DCP_Auto charging mode per below table. When system is put back to operation mode then set control pins to correspond to SDP or CDP mode and so on.

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I_{OS_PW} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP _Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP	ILIM_HI	OFF	
1	1	1	0	SDP(4)	ILIM_LO	OFF	
1	1	1	1	CDP(4)	ILIM_HI	CDP load present(5)	Data Lines Connected and Load Detect Active

(1) TPS2543 : Current limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the “Load Detection – Power Wake” limits.
(3) DCP Load present governed by the “Load Detection – Non Power Wake” limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) CDP Load present governed by the “Load Detection – Non Power Wake” limits and BC 1.2 primary detection.

Table 3 can be used as an *aid* to program the TPS2543 per system states however not restricted to below settings only.

Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2543 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

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Load Detect

TPS2543 offers system designers unique power management strategy not available in the industry from similar devices. There are two power management schemes supported by the TPS5243 via the STATUS pin, they are:

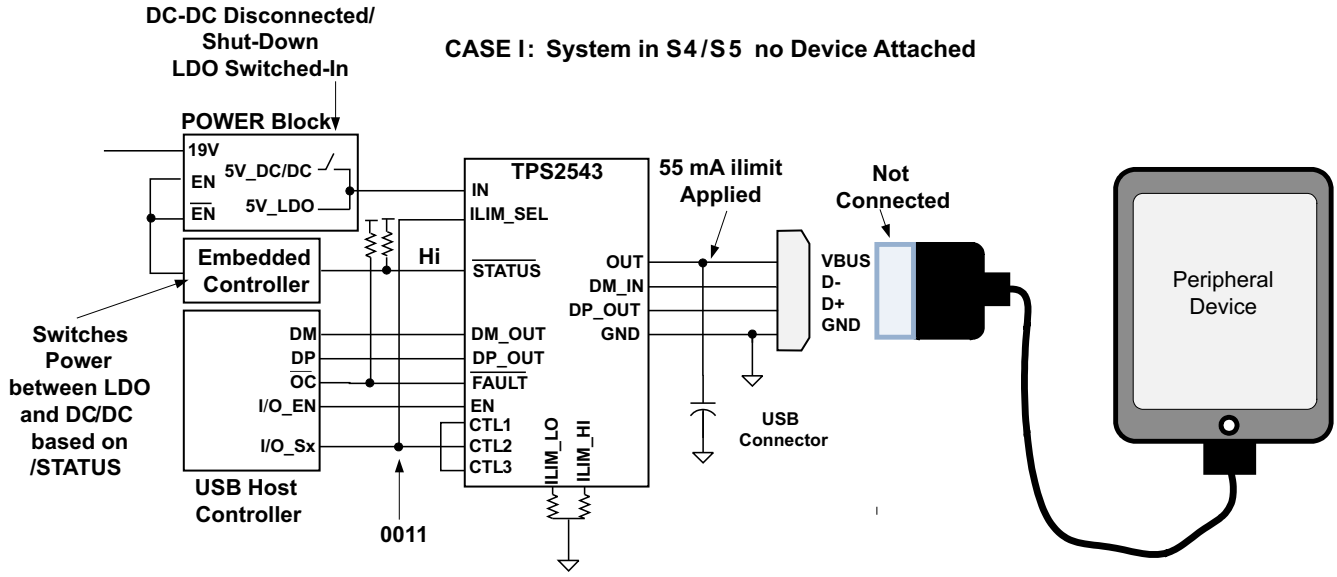
1. Power Wake (PW)
2. Port Power Management (PPM)

Either feature may be implemented in a system depending on power savings goals for the system. In general Power Wake feature is used mainly in mobile systems like a notebook where it is imperative to save battery power when system is in deep sleep (S4/S5) state. On the other hand Port Power Management feature would be implemented where multiple charging ports are supported in the same system and system power rating is not capable of supporting full charging on multiple ports *simultaneously*.

Power Wake

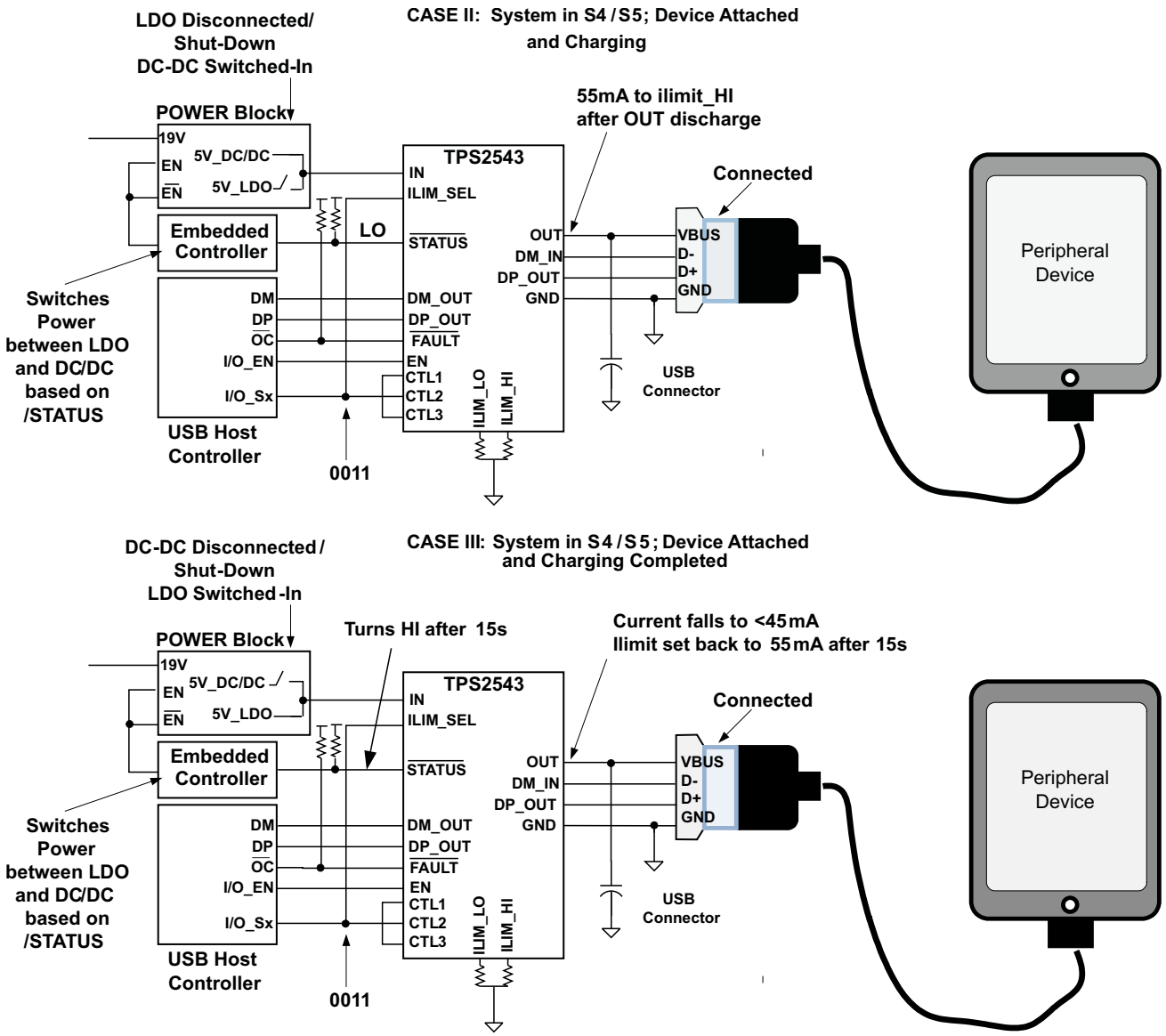
Goal of power wake feature is to save system power when system is in S4/S5 state. In S4/S5 state system is in deep sleep and typically running of the battery; so every “mW” in system power savings will translate to extending battery life. In this state the TPS2543 will monitor charging current at the OUT pin and provide a mechanism via the STATUS pin to switch-out the high power DC-DC controller and switch-in a low power LDO when charging current requirement is <45mA (typ). This would be the case when no peripheral device is connected at the charging port or if a device has attained its full battery charge and draws <45mA.

As shown in below when system is in S4/S5 mode (0011 setting, see device truth table) and no device is connected to the charging port (Case I) system runs off a 100mA LDO. Also note TPS2543 will automatically set its ilimit to 55mA (typ) irrespective of ILIM_LO and ILIM_Hi setting.



Now when a device is attached (CASE II) and draws >55 mA of charging current the TPS2543 will hit its internal current limit as the current drawn by the attached device will exceed the 55mA ilimit threshold. This will trigger the device to assert STATUS to turn on the main power supply and discharge OUT for 310ms (typ) to allow the main power supply to turn on. After the discharge the device will turn back on with current limit set by ILIM_HI. In Case III as the attached device is being charged the TPS2543 will monitor its load current. STATUS remains asserted until load current drops below 45mA (typ) for a continuous period of 15s indicating that the attached device is fully charged. At this point STATUS de-asserts and ilimit is set back to 55mA as shown below.

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Port Power Management

Port power management is for systems that have multiple charging ports but cannot power them all simultaneously. Goal of this feature is two fold:

1. Enhances user experience since user does not have to search for charging port
2. Power supply only has to be designed for a reasonable charging load

All ports are allowed to broadcast high current charging, charging current limit is based on ILIM_HI resistor setting. System monitors $\overline{\text{STATUS}}$ to see when high current loads are present. Once allowed number of ports assert $\overline{\text{STATUS}}$, remaining ports are toggled to a non-charging port. Non-charging ports are SDP ports with current limit based on ILIM_LO. TPS2543 allows for a system to toggle between charging and non-charging ports either with an OUT discharge or without an OUT discharge.

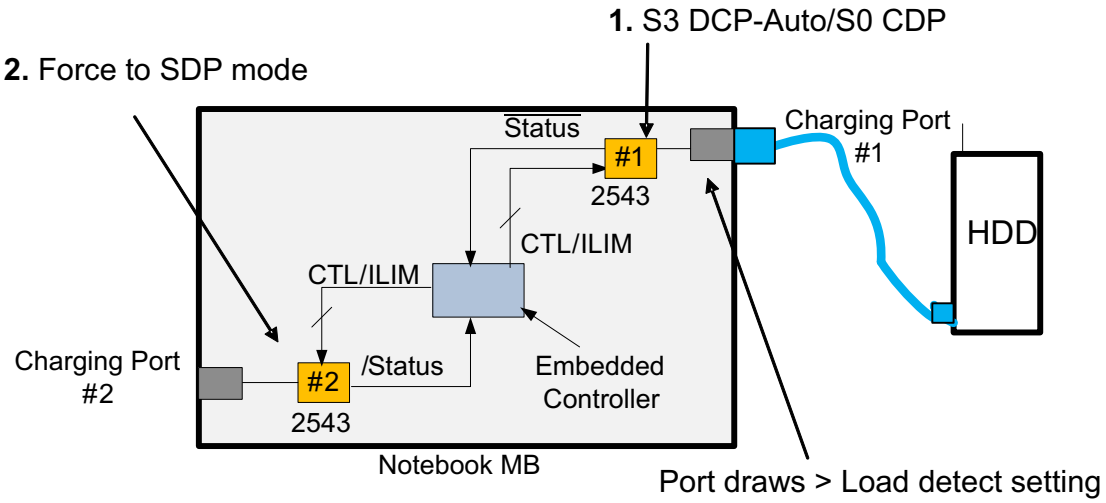


Figure 33. Implementing Port Power Management in a System Supporting Two Charging Ports

Over-Current Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied. The TPS2543 senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 20°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

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Current-Limit Settings

The TPS2543 has two independent current limit settings that are each programmed externally with a resistor. The ILIM_HI setting is programmed with R_{ILIM_HI} connected between ILIM_HI and GND. The ILIM_LO setting is programmed with RILIM_LO connected between ILIM_LO and GND. Consult the Device Truth Table (Table 2) to see when each current limit is used. Both settings have the same relation between the current limit and the programming resistor.

R_{ILIM_LO} is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use R_{ILIM_LO} < 80.6 kΩ.

The following equation programs the typical current limit:

$$I_{OS_typ}(mA) = \frac{50{,}500}{(R_{ILIM_XX}(k\Omega) + 0.1)} \quad (1)$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

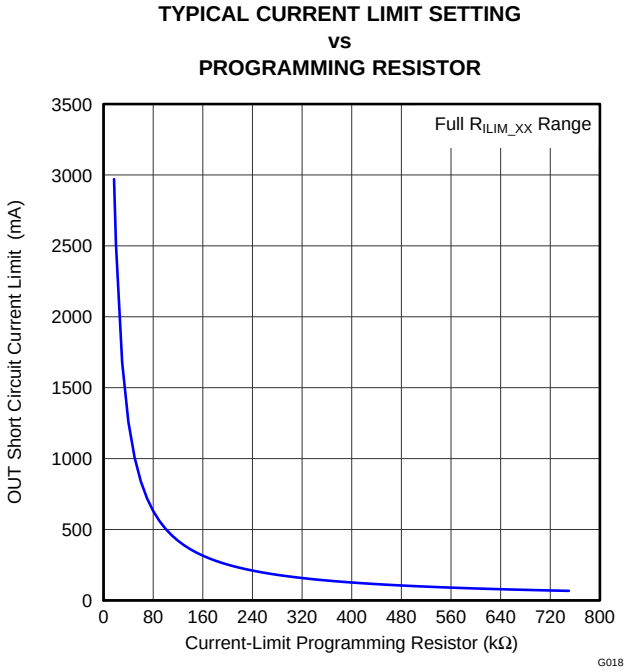


Figure 34.

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Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS2543 current limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the TPS2543 minimum / maximum current limits to within a few mA and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal - no variation - external programming resistor. To take resistor tolerance into account, first determine the minimum / maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the programming resistor, use the maximum resistor value in the I_{OS_min} equation and the minimum resistor value in the I_{OS_max} equation.

$$I_{OS_min}(mA) = \frac{45{,}661}{(R_{ILIM_XX}(k\Omega) + 0.1)^{0.98422}} - 30 \quad (2)$$

$$I_{OS_max}(mA) = \frac{55{,}639}{(R_{ILIM_XX}(k\Omega) + 0.1)^{1.0143}} + 30 \quad (3)$$

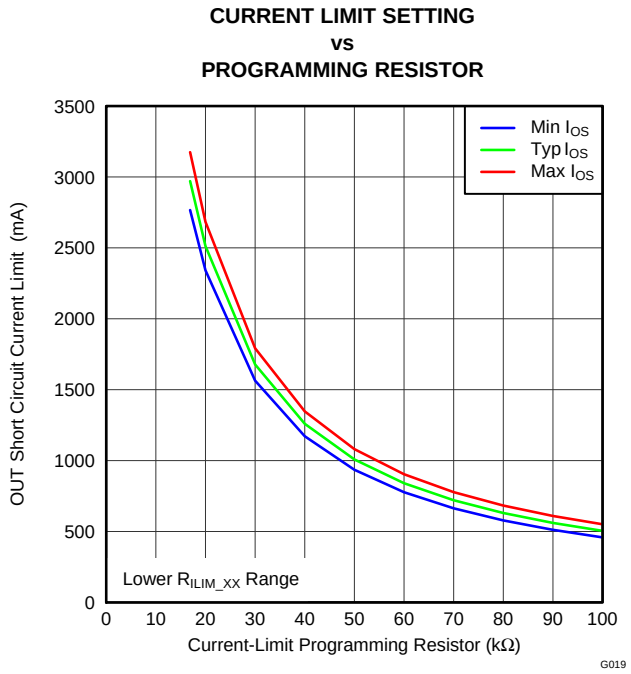


Figure 35.

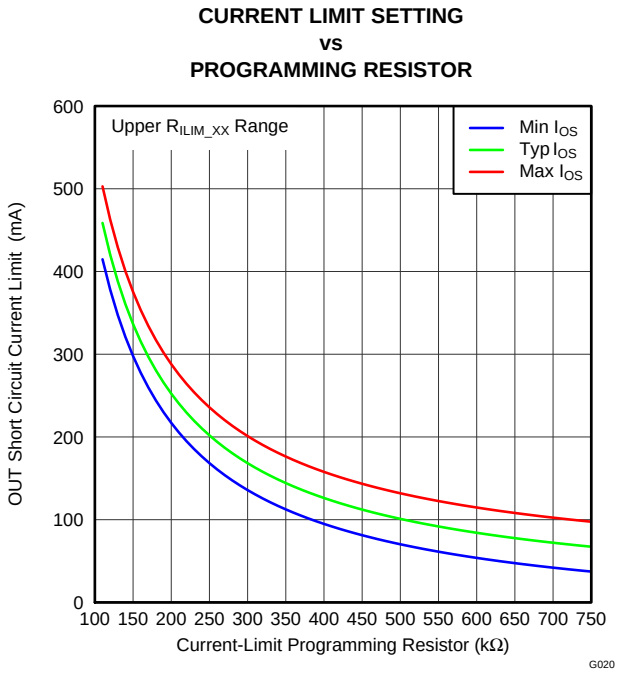


Figure 36.

The traces routing the R_{ILIM_XX} resistors should be a sufficiently low resistance as to not affect the current-limit accuracy. The ground connection for the R_{ILIM_XX} resistors is also very important. The resistors need to reference back to the TPS2543 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS2543 GND pin.

FAULT Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-temperature or current limit condition. The output remains asserted until the fault condition is removed. The TPS2543 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

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Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

The TPS2543 protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the part is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output $\overline{\text{FAULT}}$ is asserted (active low) during an over-temperature shutdown condition.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2543RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2543RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

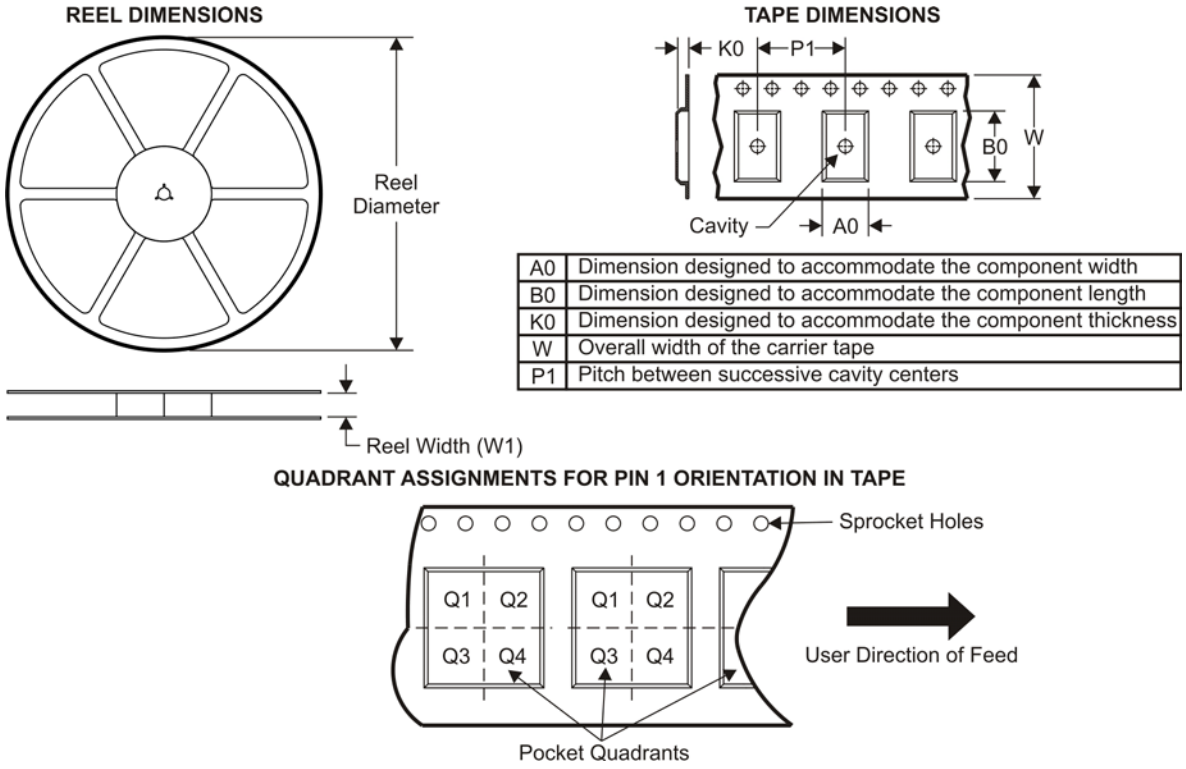
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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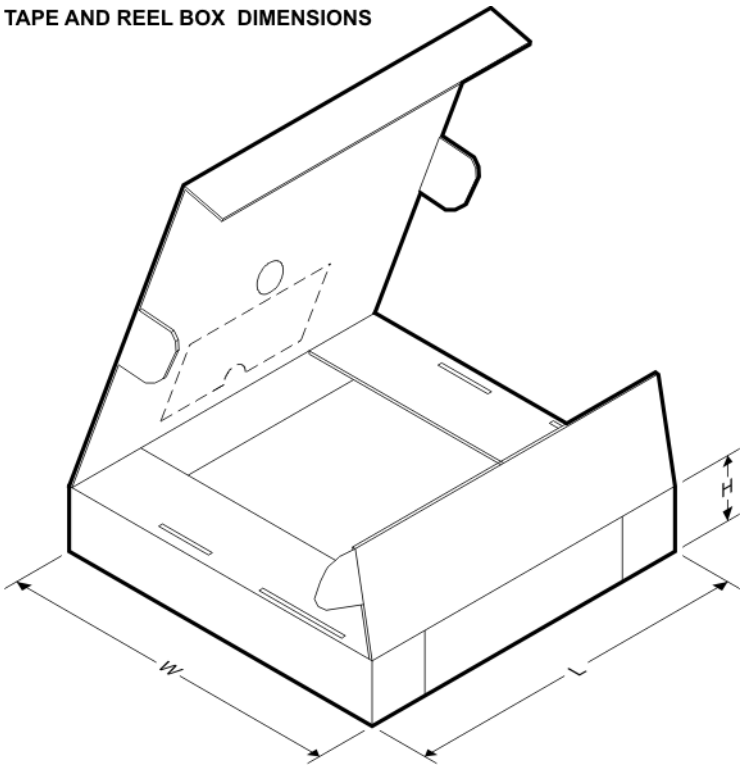


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2543RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2543RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	13.0	Q2

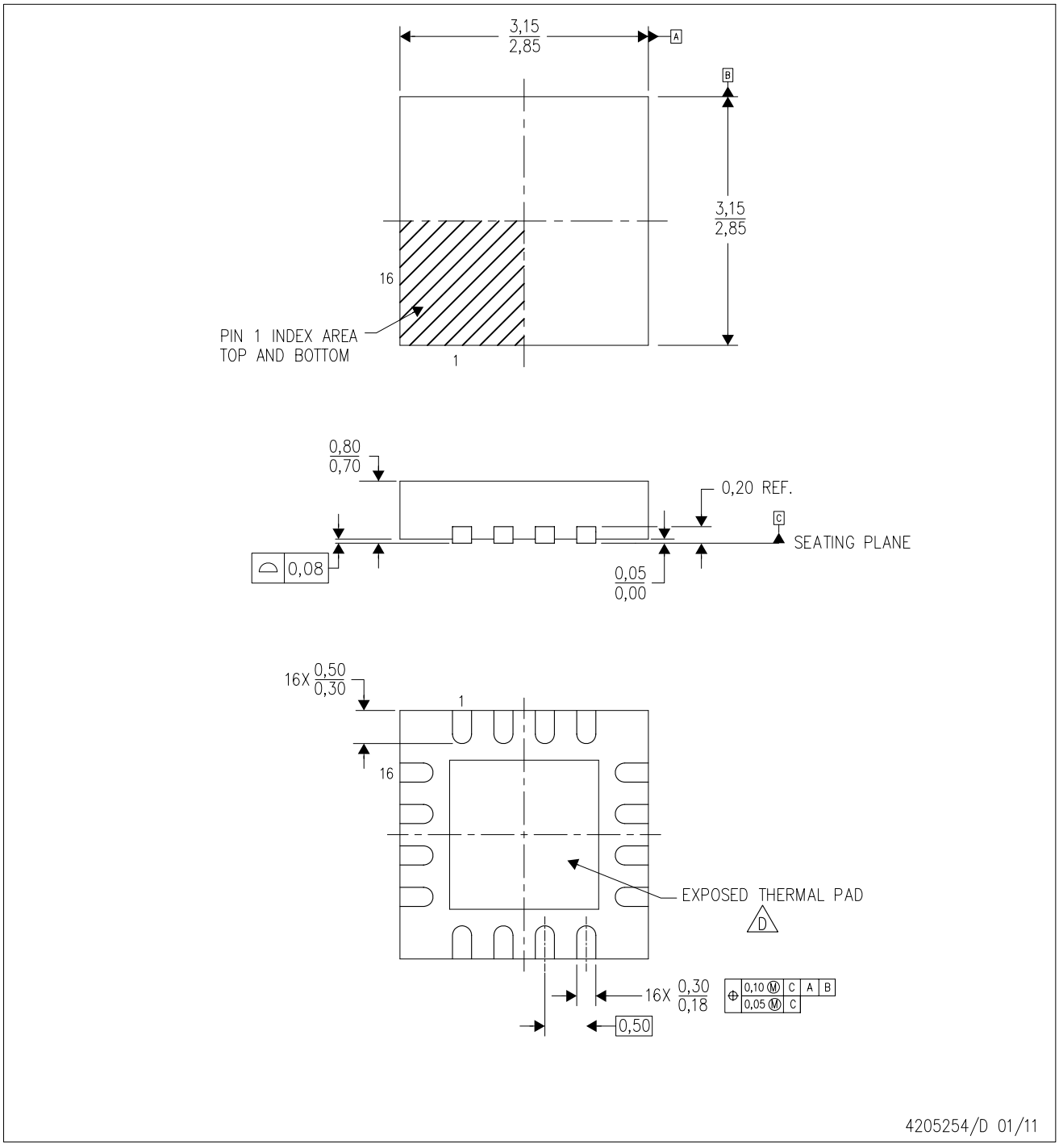
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2543RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2543RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

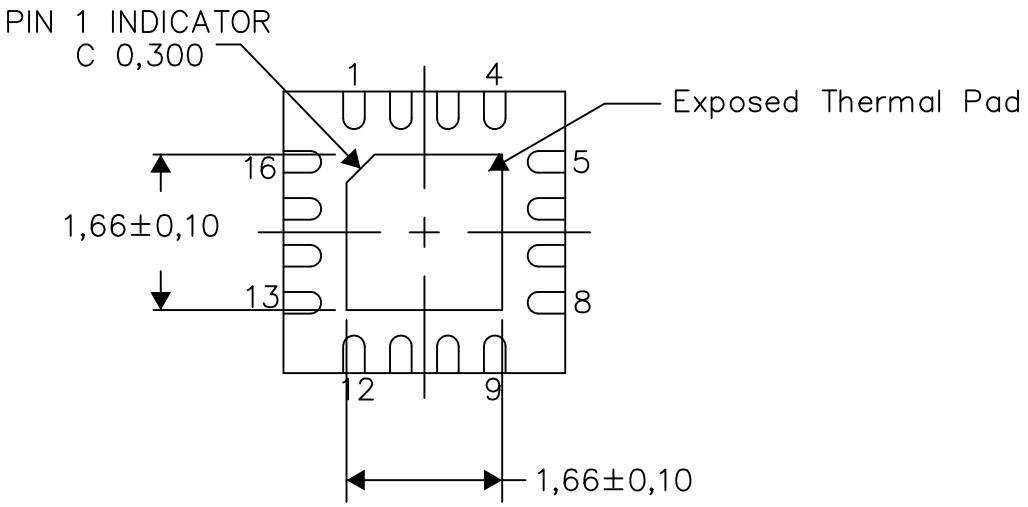
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



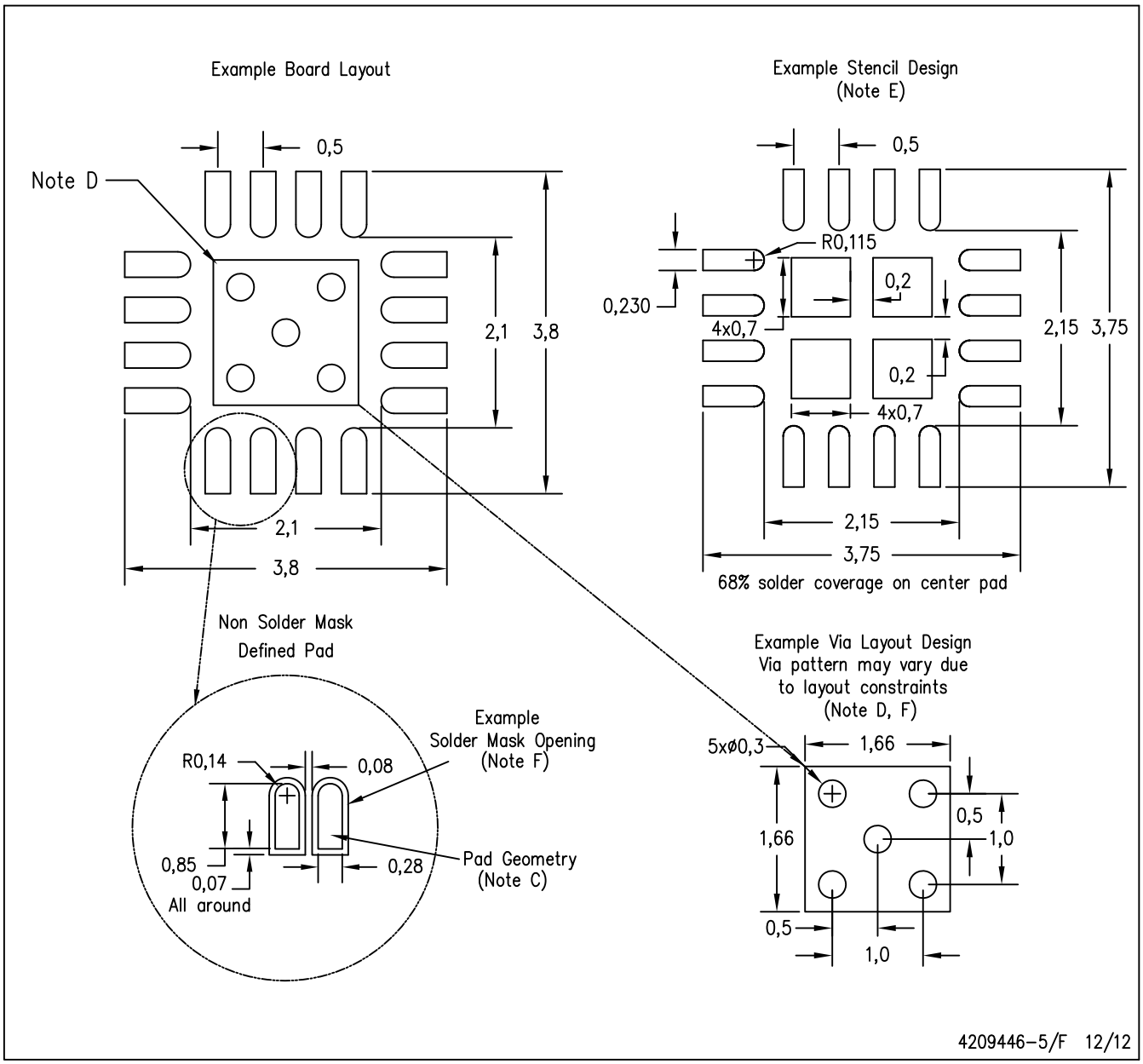
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/K 12/12

NOTE: A. All linear dimensions are in millimeters

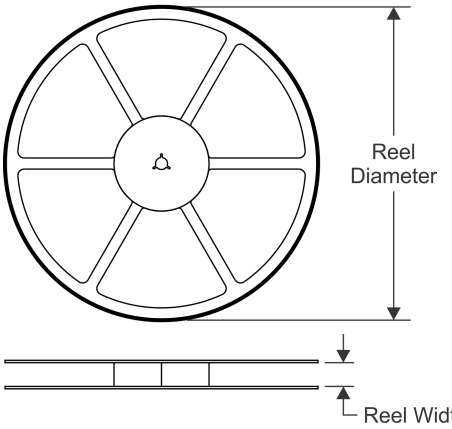
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



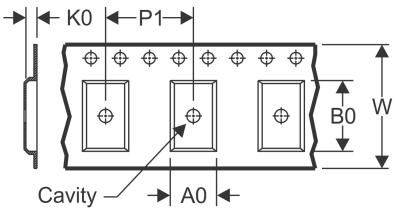
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

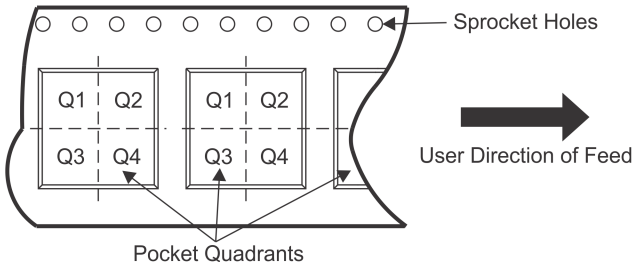


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
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P1	Pitch between successive cavity centers

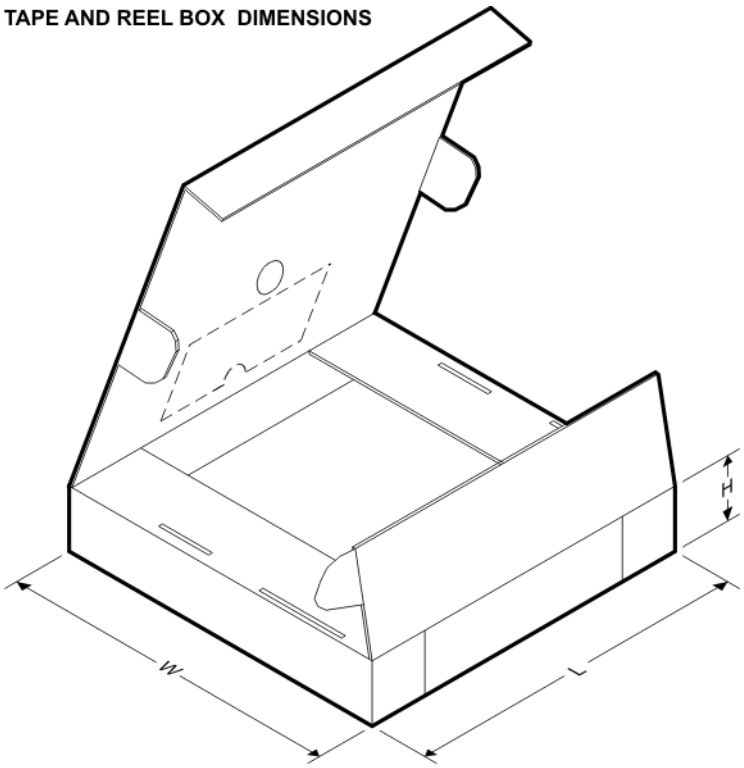
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2543RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2543RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2543RTET	WQFN	RTE	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2543RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2543RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2543RTER	WQFN	RTE	16	3000	338.0	355.0	50.0
TPS2543RTET	WQFN	RTE	16	250	338.0	355.0	50.0
TPS2543RTET	WQFN	RTE	16	250	210.0	185.0	35.0

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